ECE 404 Honors Option
Two-Stage Low-Noise RF Amplifier Circuit Design

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***Abstract*—This project was to design and fabricate a two-stage low-noise RF amplifier using both transmission lines and lumped components. This paper will discuss the matching methodology used for this two-stage amplifier, as well as discuss how software can assist in RF design. In addition to explaining the software simulations that were performed, an explanation of the necessary hand calculations for this particular design are also presented on. The results of the fabricated design will be presented, as well as a discussion of some of the immediate altercations add improvements that were made to the design. An analysis of the pros and cons of these altercations is conducted, supported by measurements and graphs that characterize the device. To finish, this paper will discuss further improvements that can be made to the design, as well as briefly reflect on other design decisions that could have been made. Referencing this paper, readers should be able to design their own two-stage low-noise RF amplifier if they have a basic understanding of RF and circuit design.**

I. Introduction

Something to keep in mind is that the biasing conditions of the transistor are very important. The transistor that this project uses is the BFU730FNPN, wide band silicon germanium RF transistor, from NXP Semiconductors. The base current and collector emitter voltage of this device will determine the collector current. In this RF application, there will be a constant amplification of DC across the device, and then the RF signal, transposed over the DC, will be amplified as well. Filtering out the DC at the input and output of the device will mean that we can isolate only the RF signal, which is what we will do in this project.

Low-noise amplifiers, or LNAS, are important tool in the area of RF. LNAs are used for a variety of applications. The most common application is in receiver systems where amplifying a weak signal is required, as well as filtering out unwanted frequencies [1]. LNAs attempt to amplify a signal while adding minimal noise to the system.

The driving devices of LNAs are most commonly junction field-effect transistors, RF transistors, or high-electron-mobility transistors. These semiconductor based devices have high switching and a reliable gain, leading to stable, high performing, LNAs. Each one of these devices has a maximum achievable gain, based on the voltage and current at terminals of the device. If a particular device cannot produce desired gain with standard 50-Ohm terminal matching, modifying the input and output matching networks of the device can sometimes lead to improved gain, while maintaining or even improving upon performance with respect to low-noise and stability. If a device, with matching, cannot produce the desired gain, then it sometimes becomes necessary to create a system that chains multiple amplifying devices together in series. The gains of each device compounds, and the desired gain, which was previously not achievable, becomes achievable. Amplifiers that make use of multiple amplifying devices are called multistage-stage amplifiers. Multi-stage amplifiers have an increased complexity, as each device requires an input and output matching network, as well as a baising network, but they are sometimes necessary to meet the specifications of a LNA or other systems. For this LNA design, we will use a two-stage design, using two amplification devices, which is required in order to achieve our target 30 dB gain.

Another thing to keep in mind when designing multi-stage LNAs, or even single-stage LNAs is that the amplifying device in the system amplify both signal and noise at the input, and themselves add a little bit of noise to the output. This means it is important to try to minimize noise at the input of the LNA, but as with many things, there is a balancing that must take place.

For LNA design, the matching of each amplifying device will determine the stability, gain, and noise characteristics of the overall design [2]. This matching is device specific, based on the S-parameters at varying DC biasing of the amplifying device. The two-stage amplifier design that will be discussed in this paper uses two BFU790FNPN, wide band silicon germanium RF transistors, from NXP Semiconductors. Although the biasing of each transistor used here is specific to these particular transistors, the design principles discussed here can be generally applied to many amplifying devices used in LNA design.

Another important facet of LNA design is isolating RF signals as inputs and outputs, and ensuring that the transistor biasing is strictly DC [2]. This is achieved though using DC blocking capacitors at the input of the device, and DC feeding inductors at the biasing DC pads of the device. The DC blocking capacitors are usually as simply as chaining the DC capacitors in series at the input and output of the device. Isolating any RF from the biasing tends to be a more difficult procedure, as the DC feeding inductor tends to

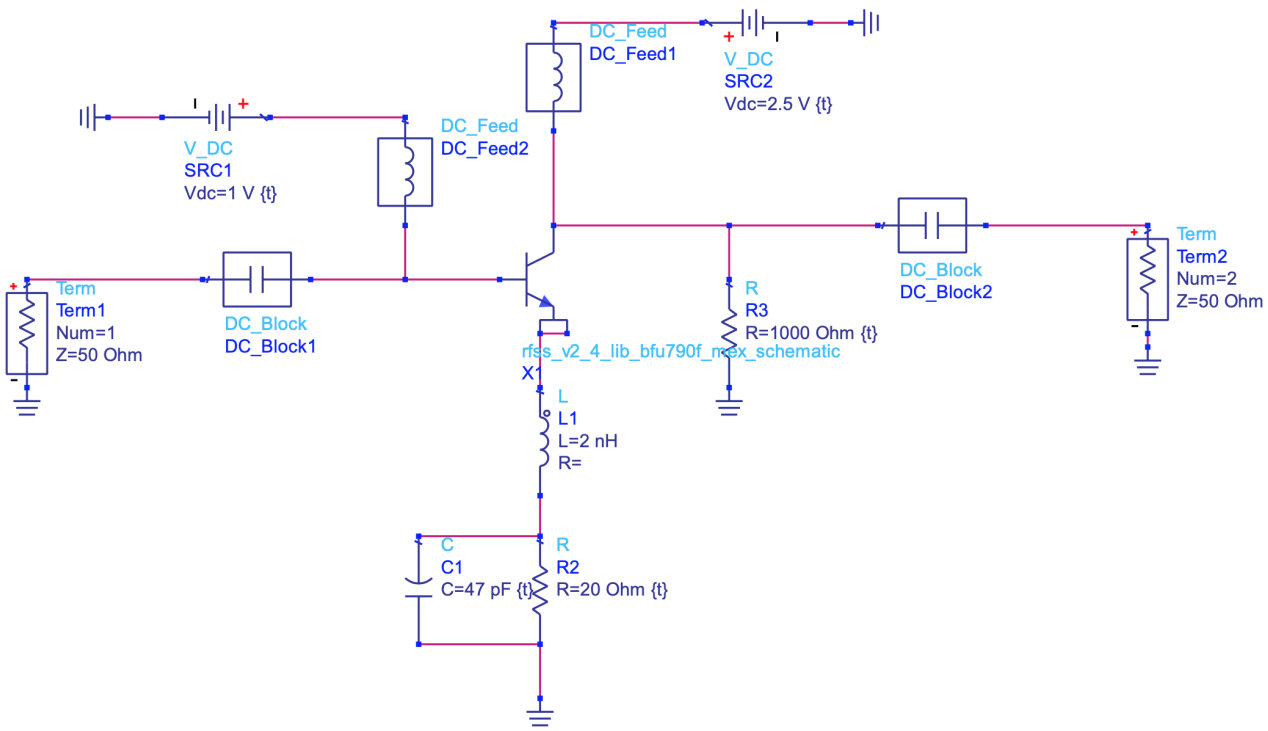

Fig. 1. Designed matching network in ADS of a single transistor for stability, noise, and gain.

want to oscillate with any stray capacitive loads. This paper will discuss some attempts to minimize oscillation at the DC inputs, in addition to simply making use of a DC feeding inductor in series.

II. Design

Major design considerations of an LNA can all be made via a Smith chart. For this project, the center frequency, of amplification was to be 915 MHz, the gain (S_{21}) was desired as greater than 30 dB at this target frequency, both S_{11} and S_{22} had to be less than -8 dB at the target frequency, the device had to be unconditionally stable over a wide frequency range, and the design had to fit within a substrate area of 2.5" X 2.5". There was no explicit requirement for a noise factor, but a noise factor of less than 1.5 dB was aimed for in design.

A. Design Basics

This design required two transistors to meet the project requirements. Since 30 dB was desired, each transistor and its matching network was to put out 15 dB of gain. The two chained together should produce 30 dB of gain for the entire device. Using Advanced Design System (ADS) by Keysight Technologies, we first created a basic biasing network for a single transistor. From there, we added a stabilization resistor in parallel at the output of the transistor in order to help stabilize it.

Additionally, since the pad that the transistor is mounted to on the physical board caries an inductance to it, we added an inductor in series with the emitter of the transistor and ground it a modeling transistor in hopes to better understand the real devices stability in our design. We found that adding an additional stabilizing resistor in series with the modeled inductor and ground lead to increased stability. Since we only wanted this stability at higher frequencies, we put in parallel to that resistor a capacitor. This means that the stabilization resistor has more influence at lower frequencies than at higher frequencies, as the capacitor behaves as a short circuit at higher frequencies, bypassing the resistor, and an open circuit at lower frequencies, maximizing the influence of the resistor. In a previous project, we found that the device was stable at higher frequencies than lower frequencies, and this is why this low frequency stabilization configuration at the emitter side of the transistor was included. If there was no inductance at the collector of the transistor, our device would be much more stable, but there was not much that we could easily do to minimize this. One solution we knew was chaining multiple vias on the small mounting pad of the collector, but this was difficult and would only minimize the inductance. Hence, we simply aimed to design for a significant inductance at the collector, and hoped that the inductance of the pad was actually less than we designed for, with the plan to minimize that inductance is needed after the board was printed. The

basic biasing network with all of its components can be seen in Fig. 1.

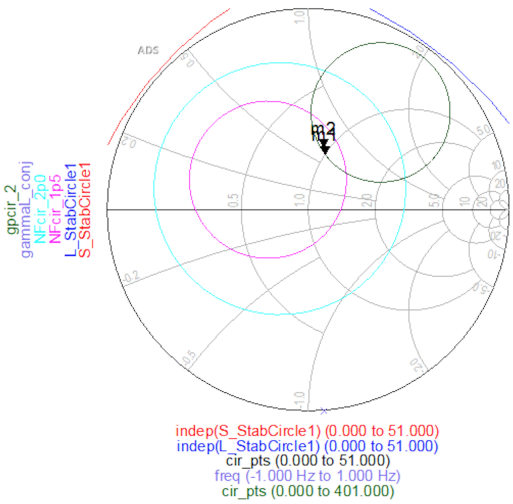

Fig. 2. The Smith chart for the transistor biasing network.

The values of the components found in Fig. 1 were all tuned for optimized performance with respect to stability, noise, and gain in Fig. 2. The red and blue lines on the schematic are the input and output stability circles. The green circle is the 15 dB available power gain G_A circle, with m1 being the chosen point on the gain circle for matching, with m2 showing the conjugate match at the output. The pink circle is the noise factor circle at 1 dB and the cyan circle is the noise factor circle at .6 dB. This was the best performance we are able to achieve with the given transistor, and this was with biasing of V_{CE} of 2.5 V and a V_{EB} of 1 V. m1 could be any point on the G_A circle [3], and m2 would vary based on that value. Using ADS, m1 was picked so that matching both m1 and m2 would be simple. As seen in figure Fig. 2, matching m1 and m2 should be easy as they are both close to the Smith chart center. A discussion of the G_A circle, and how m2 was calculated after m1 was selected can be found in the Design Calculations portion of this report.

For this design we decided to to use the the G_A circle and conjugate match the output for a few reasons. First, it would minimize noise in the system, as our input matching would be flexible. We would be able to match anywhere on the G_A circle, and chose a point for minimum noise, maximum bandwidth, maximum stability, and also chose a point that can be easily matched. Again, the noise from the output matching is much less relevant to the total noise from the transistor, as this noise is not amplified by the transistor itself like the input noise would be. Another reason for conjugate matching at the output is because it means that chaining multiple transistors becomes much simpler. We do not have to do any complex matching for our chained transistors - we simply need to copy and paste. This is because the output is matched to the center, and we are chaining transistor networks with 15 dB gain. As the transistor networks are identical, input matching and output matching for all transistors is identical. This means that we can simply chain our 15 dB transistor network with one another to get 30 dB gain. Additionally, as we designed for optimal noise at the input, this is the lowest noise possible for the entire system. Another benefit to using available power gain and conjugate matching the output to the Smith chart center is that we are able to add a DC blocking capacitor in between transistor networks without altering the input matching. This DC blocking capacitor is extremely important, since it prevents the DC voltage (V_{CE}) from the collector-emitter biasing of the previous transistor from leaking into the next. If we did not output match to center, we would have to build this DC blocking into our input network; matching at center means we have much more flexibility in DC blocking and the capacitor that we use.

After determining what points we needed to match to, indicated by m1 and m2 in Fig. 2, we needed to actually come up with our input and output matching. The points m1 and m2 were chosen with simple matching in mind. For input matching to m1, only a single inductor was needed. The value of this inductor is 2.4 nH, calculated at center frequency. Matching to m2 also required a very simple matching network of the 1000 Ohm stabilization resistor in parallel at the transistor output, collector by a 3 nH inductor.

From there, all the transmission lines were added to the schematic, required to collect lumped elements. The vias were included, as well as the DC blocking capacitors and the pad layout for the transistor. We then copied and pasted this single transistor network so that we had two, giving us our desired 30 dB total gain. The only thing left to add then was our DC pads for biasing each transistor. Our DC pads included a large inductor between them and the transistor, isolating RF from the DC source, and a grounded capacitor, helping to stabilize the pad to a single voltage. We found that this simple pad wasn't enough to prevent loading the network and having oscillations, but this will be discussed later in the paper. After including our DC pads, the design was complete. The final design can be seen in Fig. 3 on the following page.

B. Design Calculations

ADS handled the majority of the computations for us, but it is important to know what operations ADS used and how we came up with our design more conceptually.

The G_A circle was computed in ADS, but can be computed by hand as well. The center of the G_A circle, known as C_A, follows:

$$C_A = g_A C_1^* / 1 + g_A(|S_{11}|^2 - |\Delta|^2) \quad (1)$$

[3].

where g_A, the normalized gain, is the desired gain, G_A, over the transistor gain, $|S_{21}|^2$.

$$g_A = G_A / |S_{21}|^2$$

[3].

where

$$C_1 = S_{11} - \Delta S_{22}^* \quad (2)$$

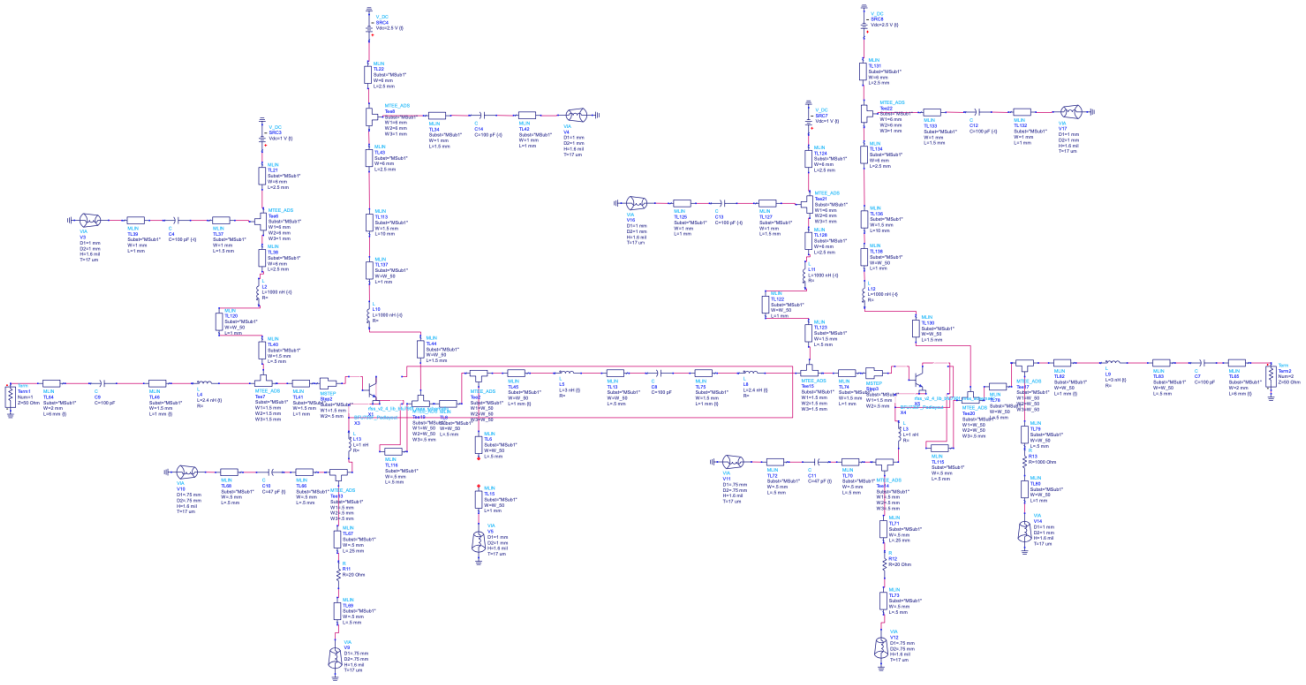

Fig. 3. Our finalized design in ADS, including all lumped elements, transmission lines, DC pads, vias, etc.

[3].
and

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3}$$

[3].
The radius of G_A circle, represented by R_A, can be computed by:

$$R_A = [1 - 2Kg_A|S_{12}S_{21}| + g_A^2|S_{12}S_{21}|^2]^{(1/2)} + /|1 + g_A(|S_{11}|^2 - |\Delta|^2)| \tag{4}$$

[3].
where

$$K = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2)/(2|S_{12}S_{21}|) \tag{5}$$

[3].
As mentioned earlier, we selected a point on this gain circle, Γ_S, and then using that point, we found Γ_L by conjugate matching, using:

$$\Gamma_L* = \Gamma_{OUT} = [S_{22} + (S_{12}S_{21}\Gamma_S)/(1 - S_{11})\Gamma_S] \tag{6}$$

[3].
The equations for Δ and K are important, as they are also used in verifying the stability of the design, which will be explored in the following section.

The center of the noise figure circles were determined by:

$$C_{F_i} = \Gamma_{opt}/(1 + N_i) \tag{7}$$

[3].
and the radius by:

$$r_{F_i} = (N_i^2 + N_i(1 - |\Gamma_{opt}|^2)^{1/2}/(1 + N_i) \tag{8}$$

[3].
where Γ_{opt}, r_n, and F_{min} are called noise parameters, and are provided by the devices manufacturer, and N_i is defined by:

$$N_i = (F_i - F_{min})/(4r_n) \tag{9}$$

[3].
where F_i is the desired noise.

Note that these by hand calculations correspond with the schematic in Fig. 1, accounting for each transistor network individually. There are ways to match both transistors concurrently that would use different calculations, but here we simply chained networks, as explained above [3].

C. Design Validation

After designing, it was important to make sure that our design satisfies the requirements of the project. We first verified that our gain was sufficient. The graph of the gain can be be seen in Fig. 4. As we can see in the graph, the gain

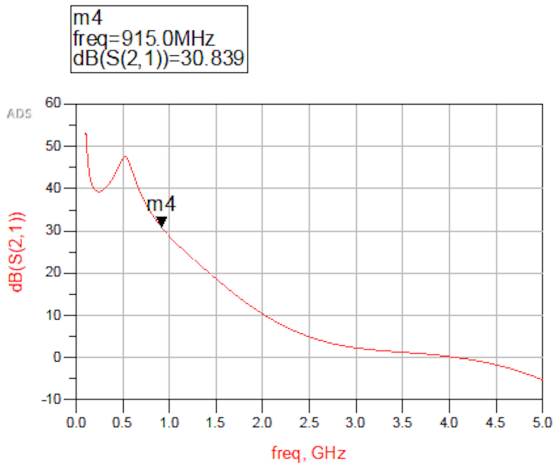

Fig. 4. The simulated gain of the LNA in ADS.

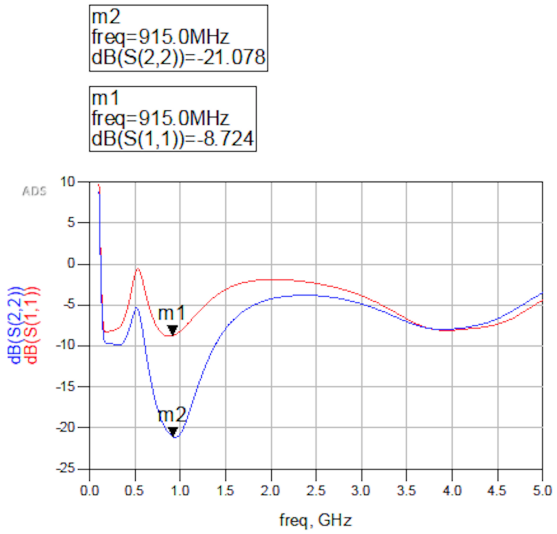

Fig. 5. The simulated S_{11} and S_{22} of the LNA in ADS.

at the target 915 MHz frequency is above 30 dB, at 30.839 dB, meeting that requirement.

Moving onto the requirement for S_{11} and S_{22} had to be less than -8 dB at the target frequency, we can see the results of the S_{11} and S_{22} at varying frequencies in the ADS simulation in Fig. 5. As shown in the figure, both are below 8 dB, meaning that this design satisfied that criteria as well.

Next for stability. Looking at the plot of K, in Fig. 6, and Δ in Fig. 7, we know that in order for the design to be stable, K must be greater than one and the magnitude of Δ to be less than one for all frequencies [3]. We see that this is true except at lower frequencies. Therefore, this design should perform well above $\sim$ 700 MHz, but perhaps struggle with respect to stability below this frequency. Although this design is not unconditionally stable at all frequencies, it is stable for a wide frequency range, and should definitely be stable at our 915 MHz center frequency.

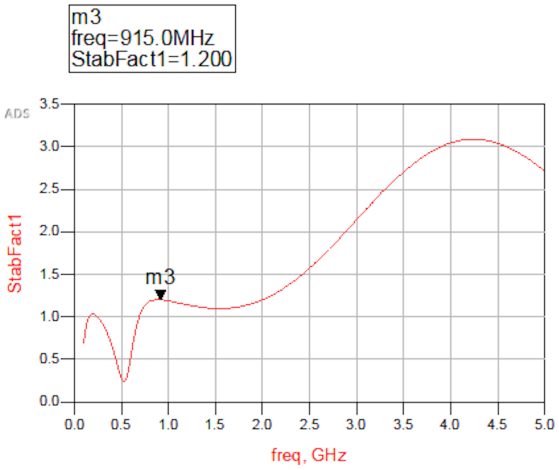

Fig. 6. The simulated K of the LNA in ADS.

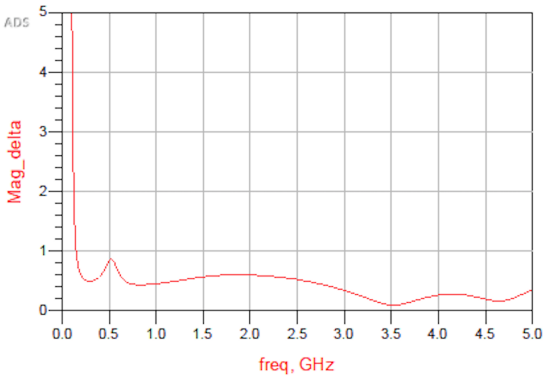

Fig. 7. The simulated $|\Delta|$ of the LNA in ADS.

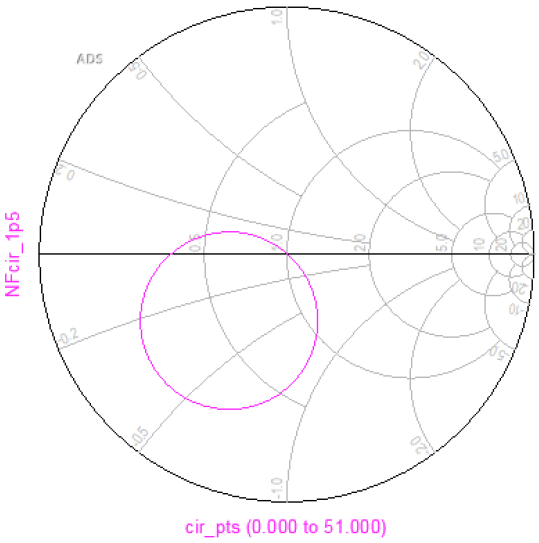

Fig. 8. The simulated noise factor of the LNA in ADS.

The last design consideration to validate is the noise of the designed LNA. Since the device is input and output matched at 50 Ohms, and the Smith chart is normalized to 50 Ohms, we know that at whatever value the noise circle intersects with the origin of the Smith chart will indicate the noise of the device. Fig. 8 shows this intersection of the noise circle with the Smith chart center. In this case, this Smith chart includes the plot of the noise figure for .49 dB of noise, which is extremely low, indicating that this LNA design is in fact low-noise. A .49 dB noise is extremely small compared to 30 dB, giving us a noise to gain ratio of $\sim$ .1%, which is very good.

III. Analysis and Discussion

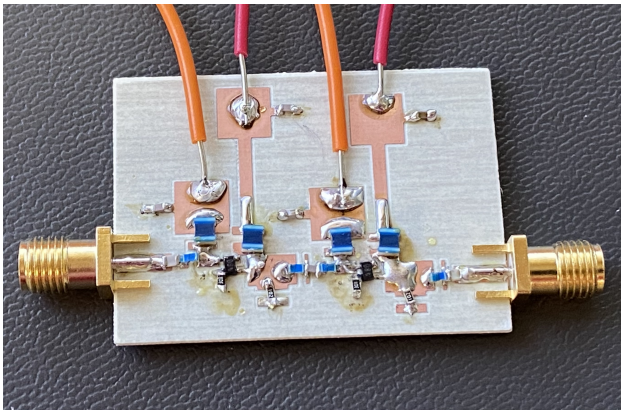

Fig. 9. The fabricated board, with all lumped components, vias, etc.

A. Fabrication and Measuring

The the copper transmission lines were fabricated, and then all lumped components soldered to the board. In addition to this, four copper lines were soldered to the four DC pads. This was simply so that it was easier to measure the characteristics of the board while maintaining a constant voltage to the DC pads. The final product can be seen in Fig. 9.

The device performance was measured using a Agilent 4396B Network Analyzer. In order to protect the Analyzer, two DC blocking ports were added to the ends of the LNA. Furthermore, the LNA was chained with two -10 dB attenuators. Both of these action ensured that the LNA could not burn or damage the Analyzer. For our graphs and data that is presented in this paper, however, due to two attenuators, all measured gain is in fact 20 dB greater than what is shown. As the attenuators are very high performing, we can assume that the attenuations are precisely -10 dB attenuation each at all frequencies.

To measure the device, we tuned the voltages for the maximum gain possible before the device becomes unstable. This occurred at V_{CE} 0f 2.30 V and V_{EB} of .97 V, very close to the V_{CE} of 2.5 V and a V_{EB} of 1 V that we designed for.

B. Initial Results

Fig. 10 shows the gain of the LNA from the original design. As seen in this figure, the gain at the center frequency slightly under performs our desired 30 dB gain with a gain of $\sim$ 26 dB. The max gain of the device is up to 35 dB, however, at a slightly lower frequency.

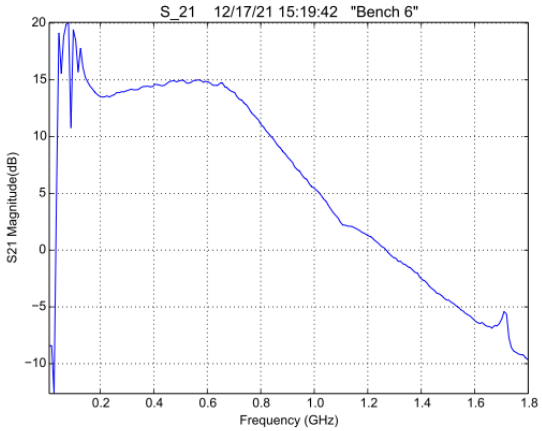

Fig. 10. The gain (S_{21}) of the fabricated design.

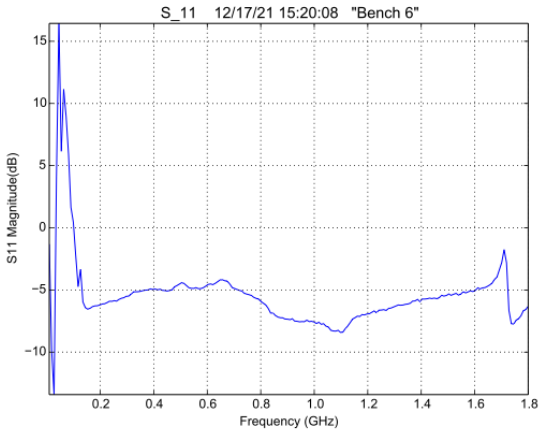

Fig. 11. The S_{11} of the fabricated design.

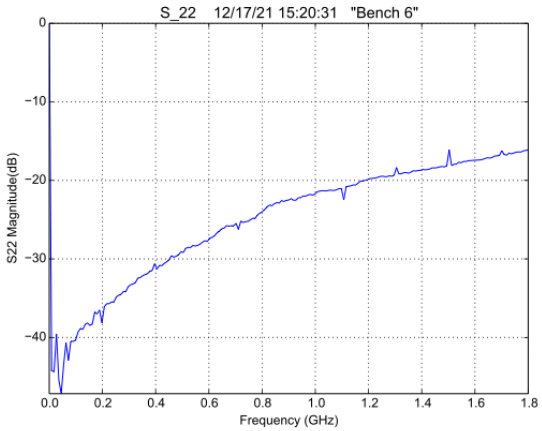

Fig. 12. The S_{22} of the fabricated design.

Looking at Fig. 11 and Fig. 12, we see that our designed S_{11} is high ($\sim$ 13 dB), and our S_{22} is also above what is acceptable ($\sim$ -2 dB).

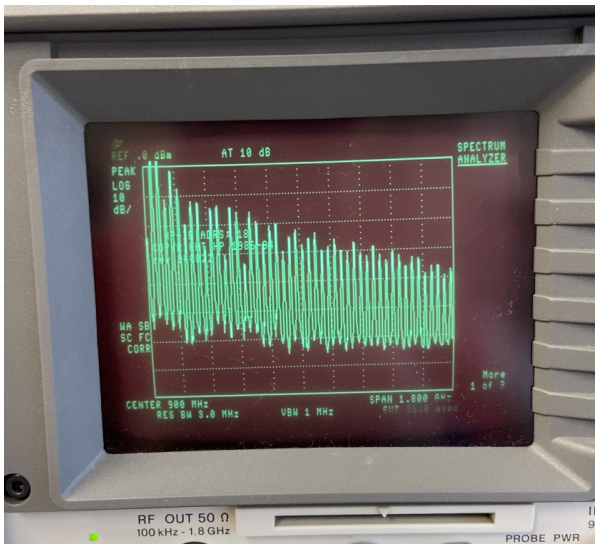

Fig. 13. The noise of the LNA measured by the spectrum analyzer.

To try to understand a little bit better of why the LNA was under performing compared to our simulations in ADS, we used a spectrum analyzer to show the noise of the LNA. This noise is shown in Fig. 13. Looking at the figure, we can see a lot of noise at lower frequencies, and still a lot, but slightly less, at higher frequencies. This indicated to us that in order for our LNA to perform well, we needed to stabilize the design better.

Furthermore, upon inspection, the DC power supply supplying V_{CE} to both of the transistors in the LNA was periodically oscillating between $\sim$ 2 V and $\sim$ 2.5 V. This is probably due to the capacitor and inductor of the DC pads oscillating. This oscillation likely led to the instability that was is seen in Fig. 13.

C. Design Altercations Aiming for Stability

1) Adding Additional Resistors at Collector Pads: In a previous project, in order to help stabilize the DC pads, we put a a 5 kilo-Ohm resistor in parallel with the DC feeding inductor. Ideally, we would have done the same here. This design unfortunately did not leave space on the board to easily place a parallel resistor, however. Therefore, we decided to place the 5 kilo-Ohm resistor in parallel with the capacitor to ground. This would achieve the same suppression of the oscillations as placing the resistor in parallel, as the oscillatory signal will dissipate across the resistor as heat. The only difference here is that having a resistor in parallel means that the power supply will have to supply more power to account for power dissipated to ground, which would not be the case if the resistor was parallel to the inductor.

After adding the two 5 kilo-Ohm resistors, we remeasured the S-parameters in order to characterize this change. This inclusion of the two resistors did suppress oscillations at the power source. Looking into the S-parameters, S_{11} at lower frequencies became slightly worse, and S_{22} was seemingly unchanged.

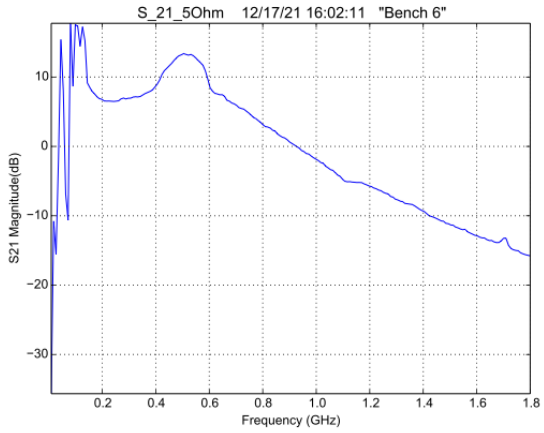

Fig. 14. The gain (S_{21}) of the fabricated design after the 5 kilo-Ohm resistors were added at the second DC pad of each transistor.

The gain was slightly decreased overall, but maintained relatively the same shape in its curve. This can be attributed to a variety of things such as some gain leaking to the added resistors or inconsistent biasing of the DC pads between tests. The biggest difference in the original S_{21} graph, seen in Fig. 10, and the S_{21} graph after the resistors were added, seen in Fig. 14, is that in the latter, there is a dip in gain at lower frequencies. This can perhaps be explained by the DC feeding inductor not fully isolating lower frequencies and the 5 kilo-Ohm resistors, in term loading the network at lower frequencies. This is reasonably related to the S_{11} at lower frequencies became slightly worse.

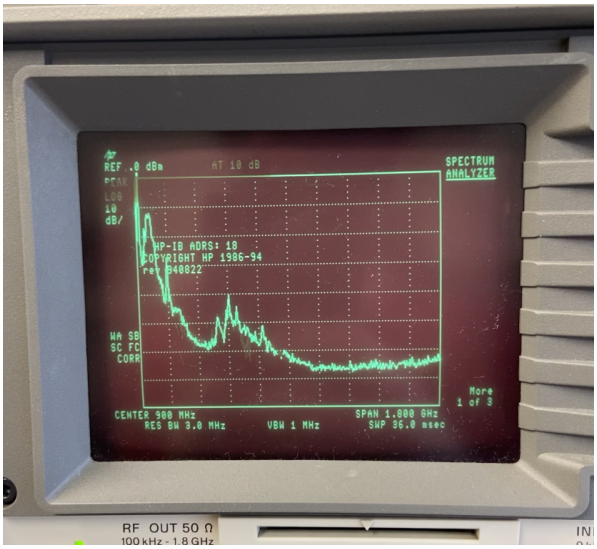

Fig. 15. The noise of the LNA measured by the spectrum analyzer with decreased V_{CE}

We next returned to the spectrum analyzer to see how this change affected the noise of the LNA. Overall, it seemed to have very little effect at the DC biasing voltages that the LNA for designed for. When we lowered the V_{CE} biasing voltage to $\sim$ 1.5V, we got the figure seen in Fig. 15. This figure does not mean too much here, as it is incomparable to Fig. 13 since the DC biasing is different, but it serves as a good anchor to compare with other altercations that occurred later on discussed below. Additionally, it emphasises the instability at lower frequencies, predicted by our simulations, and demonstrated in the figure.

2) Adding Additional Resistors at Base Pads: After adding the stabilization resistors are the collector pads, we determined that it was possible that the base pads also had oscillations leading to instability. We therefore added a parallel 5 kilo-Ohm resistor at each base pads capacitor as well. Ultimately, this had minimal affect on improving any of the S-parameters, and appeared to introduce a lot of noise into the system. This is likely because the resistors introduce noise, and if the DC feeding inductor is not entirely blocking RF noise, then the RF noise is amplified by each transistor. When working with large gains, this noise becomes a major problem for the system, which we believe to be the case here.

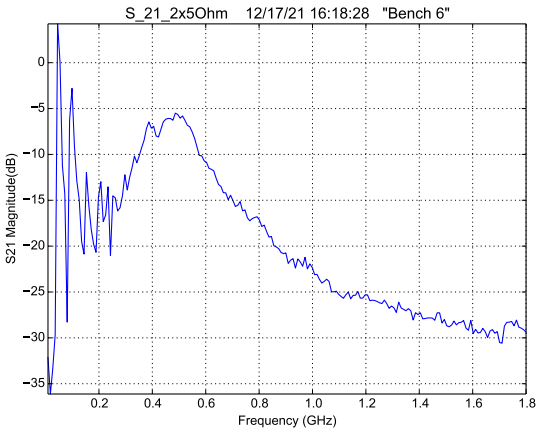

Fig. 16. The gain (S_{21}) of the fabricated design after the 5 kilo-Ohm resistors were added at the first DC pad of each transistor in addition to the second DC pads already having 5 kilo-Ohm resistors.

Fig. 16 shows the S_{21} of the device after this change was made. Comparing Fig. 16 with Fig. 14, Fig. 16 is significantly less smooth, and has even more instability at lower frequencies. This is likely due to the noise that the resistor adds. The device, in hindsight, is better off without these resistors being present at all, unless the design can better isolate RF from DC, which is appears to be struggling with. This idea is supported by Fig. 17, where there is significantly more noise at lower frequencies with the decreased V_{CE} biasing voltage from the original design. Comparing Fig. 17 with Fig. 15, it is clear that the inclusion of the resistors in this modification reduced the stability and added to the noise of the LNA.

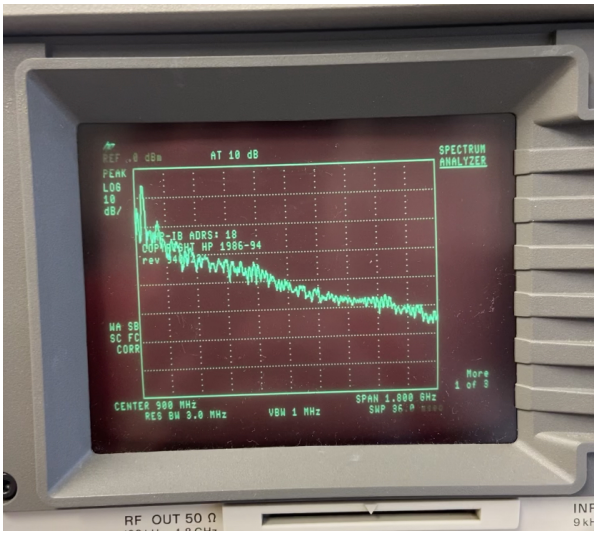

Fig. 17. The noise of the LNA measured by the spectrum analyzer with decreased V_{CE} with 5 kilo-Ohm resistors

3) Decreasing DC Feeding Inductor's Value: Further brainstorming into what could be limiting device performance brought us to the DC feeding inductors of each DC pad. The thought was that the inductor used was too large, not only adding to the resistance and capacitance of the element, but also lending itself to low-frequency oscillations. This led to switching these inductors from 1000 nH inductors to 470 nH inductors. These new inductors were smaller in both size and inductance.

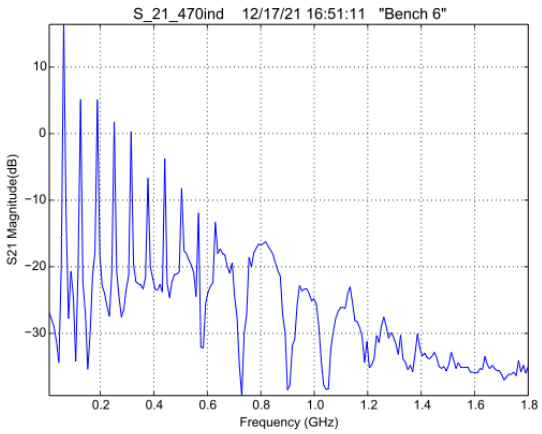

Fig. 18. The gain (S_{21}) of the fabricated design after the 5 kilo-Ohm resistors were added at the first DC pad of each transistor in addition to the second DC pads already having 5 kilo-Ohm resistors.

This change led to massive oscillations in the system. Although it slightly improved the instability at lower frequencies when visualized in the spectrum analyzer, it added to the noise at our center frequency, and created massive oscillations in our S_{21}, as seen in Fig. 18. Although it is likely that the feeding inductor is in part to blame for our devices instability and

lower than predicted gain, it is clear that decreasing the feeding inductors inductance is not a good immediate solution.

IV. Discussion and Conclusion

Despite the device not exactly meeting the design criteria or operating exactly as the ADS simulations predicted that it would, this project has been a successful demonstration of LNA design, optimized, in theory, for low-noise, stability, and high power. It is clear that the inductance of the base of the pad that the transistor's ground was soldered to in our design was still a major problem; it is likely to blame for the instability at lower frequencies, and also the power gain of the amplifier under performing. As that inductance at the emitter of the transistor increases in the simulation, the gain decreases. This is likely because the inductor draws DC from the collector of the transistors, minimizing their gain.

This transistor was difficult to stabilize to begin with, but the added inductance at the collector of the transistor made it increasingly difficult. The primary solution to this stability issue would be adding a chain of vias across the base, successively grounding it, preventing any inductance from being present. We decided not to do this originally in our design as it would be difficult to work with, however, this is probably the correct decision next time. With care, it can definitely be done, and if that inductance can be cut even in half, that would have a massive influence on the transistor being stable.

LNAs are very important in the field of RF and it is importance that this technology continues to improve so that communication systems can continue to evolve, becoming more powerful and high performing with each improvement. This project successfully demonstrated the design of a two-stage LNA, with impressive gain, minimal reflection, good stability with the exception of low frequency operation, and low-noise. The project being compact to a 2.5" X 2.5" substrate is comparable to industrial LNAs and is also quite impressive. Further improvements can be made with respect to stability and gain, and most comments on said improvements are discussed in the paper. It would also be interesting to see how using other devices, different matching methodologies, or more amplification devices, would further improve or change on the ideas presented here.

All things considered, this has been a very successful project. Many things were learned, and I have an increased confidence in RF design moving forward. Practical skills, such a soldering and trouble shooting circuits were also improved upon in this project, and I am happy to say that I have developed a very sound understanding of the material.

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